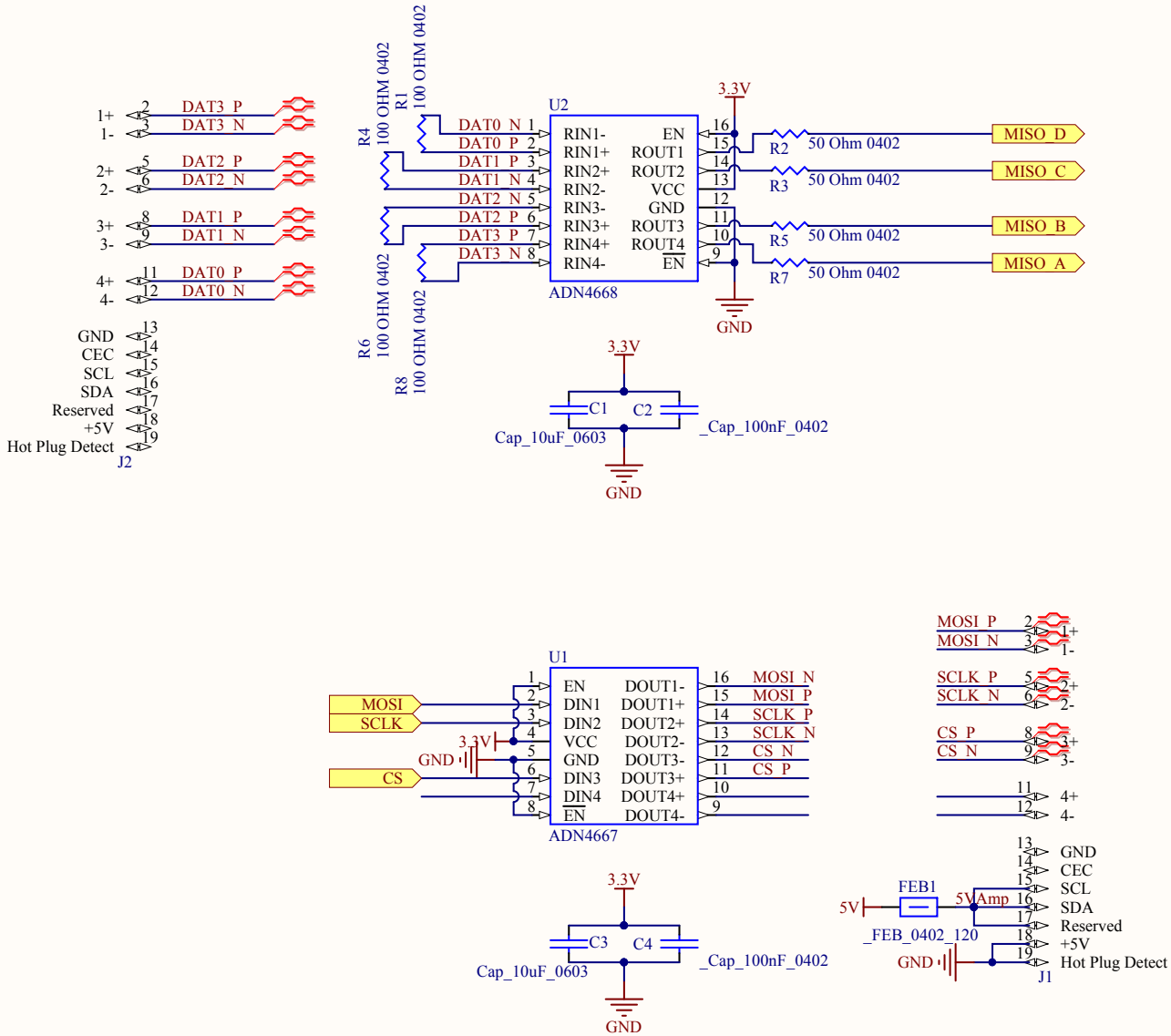

Title		
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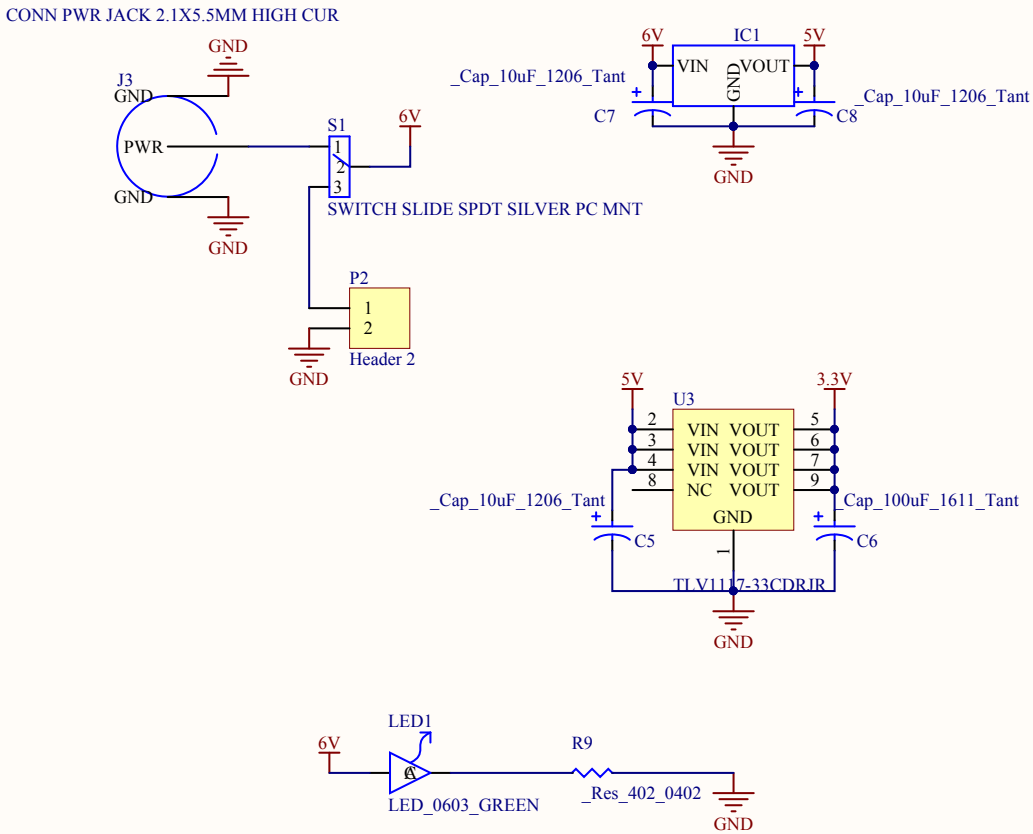
Date: 3/20/2013	Sheet of	
File: D:\Work\..\IntFPGA2.0_HdStgBlock.SchDoc	Drawn By:	



Title			
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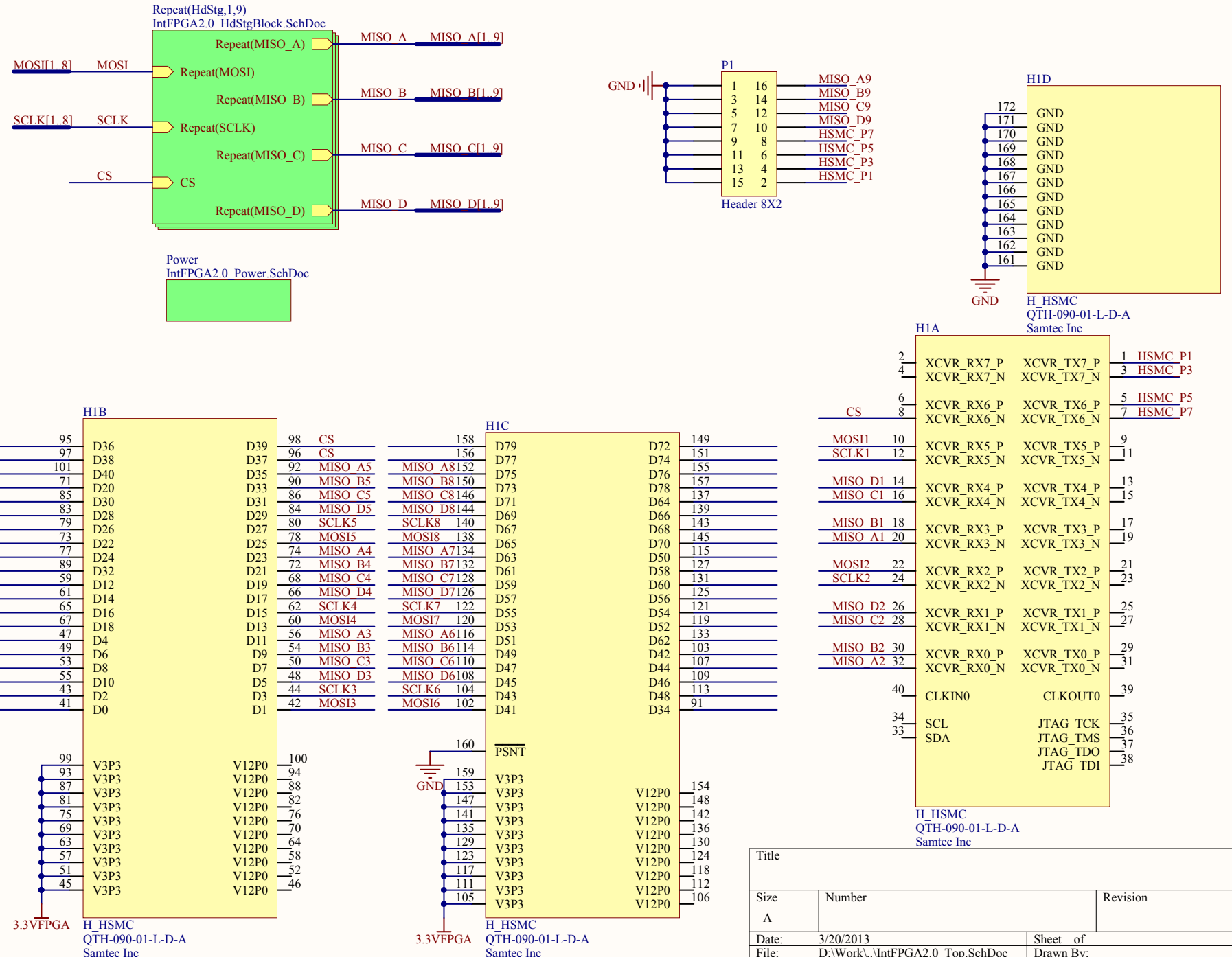
Repeat(HdStg,1,9)
IntFPGA2.0_HdStgBlock.SchDoc
Repeat(MISO_A)
Repeat(MOSI)
Repeat(MISO_B)
Repeat(SCLK)
Repeat(MISO_C)
CS
Repeat(MISO_D)
MOSI[1..8]
MOSI
SCLK[1..8]
SCLK
MISO_A
MISO_A[1..9]
MISO_B
MISO_B[1..9]
MISO_C
MISO_C[1..9]
MISO_D
MISO_D[1..9]
Power
IntFPGA2.0_Power.SchDoc
P1
GND
MISO_A9
MISO_B9
MISO_C9
MISO_D9
HSMC_P7
HSMC_P5
HSMC_P3
HSMC_P1
Header 8X2
H1D
GND
H_HSMC
QTH-090-01-L-D-A
Samtec Inc
H1A
XCVR_RX7_P
XCVR_RX7_N
XCVR_TX7_P
XCVR_TX7_N
HSMC_P1
HSMC_P3
XCVR_RX6_P
XCVR_RX6_N
XCVR_TX6_P
XCVR_TX6_N
HSMC_P5
HSMC_P7
MOSI1
SCLK1
XCVR_RX5_P
XCVR_RX5_N
XCVR_TX5_P
XCVR_TX5_N
MISO_D1
MISO_C1
XCVR_RX4_P
XCVR_RX4_N
XCVR_TX4_P
XCVR_TX4_N
MISO_B1
MISO_A1
XCVR_RX3_P
XCVR_RX3_N
XCVR_TX3_P
XCVR_TX3_N
MOSI2
SCLK2
XCVR_RX2_P
XCVR_RX2_N
XCVR_TX2_P
XCVR_TX2_N
MISO_D2
MISO_C2
XCVR_RX1_P
XCVR_RX1_N
XCVR_TX1_P
XCVR_TX1_N
MISO_B2
MISO_A2
XCVR_RX0_P
XCVR_RX0_N
XCVR_TX0_P
XCVR_TX0_N
CLKIN0
CLKOUT0
SCL
SDA
JTAG_TCK
JTAG_TMS
JTAG_TDO
JTAG_TDI
H1B
D36
D38
D40
D20
D30
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D3
D1
CS
MISO_A5
MISO_B5
MISO_C5
MISO_D5
SCLK5
MOSI5
MISO_A4
MISO_B4
MISO_C4
MISO_D4
SCLK4
MOSI4
MISO_A3
MISO_B3
MISO_C3
MISO_D3
SCLK3
MOSI3
V3P3
V12P0
3.3VFPGA
H_HSMC
QTH-090-01-L-D-A
Samtec Inc
H1C
D79
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MISO_A8
MISO_B8
MISO_C8
MISO_D8
SCLK8
MOSI8
MISO_A7
MISO_B7
MISO_C7
MISO_D7
SCLK7
MOSI7
MISO_A6
MISO_B6
MISO_C6
MISO_D6
SCLK6
MOSI6
PSNT
GND
V3P3
V12P0
3.3VFPGA
H_HSMC
QTH-090-01-L-D-A
Samtec Inc
Title
Size
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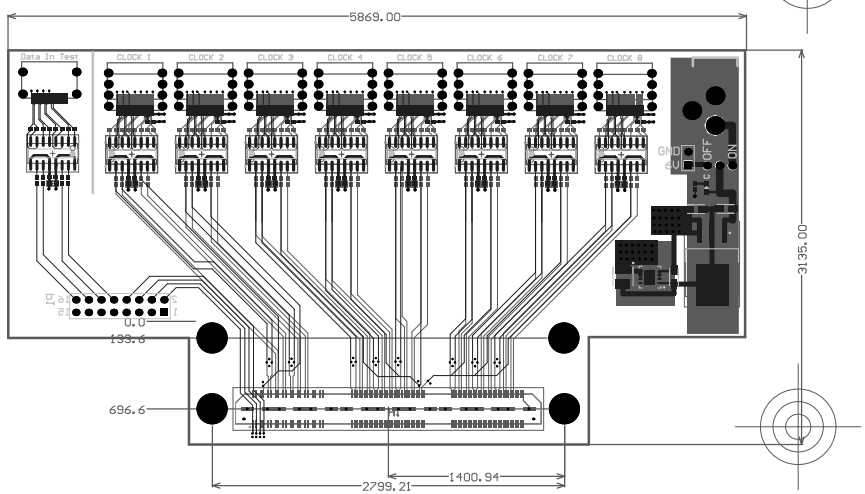
Revision
Date:
3/20/2013
Sheet of
File:
D:\Work\..\IntFPGA2.0_Top.SchDoc
Drawn By:

Layer Stack Up Detail for: Int-FPGA-Interface-2.0-Digital.PcbDoc

Layer Name
Top Side
Ground Plane
3.3V Plane
5V Plane
Ground Plane
Bottom Side



Fabrication Notes
1. Overall board height 62mils
2. 20mil pullback on inner planes
3. Tent all vias under BGA (Top Side only)
4. 1.0 Oz copper on top and bottom
5. 1.0 Oz copper on internal signal, power and ground layers

Design Notes
1. Unless otherwise stated all dimensions are in mils

LAYER - GERBER LAYERS - DESCRIPTION

GTL - TOP LAYER
GTO - TOP SILKSCREEN

GBL - BOTTOM LAYER
GBO - BOTTOM SILKSCREEN

MECHANICAL LAYERS
01 Component Outline
02 PCB BOUNDRY
03 PINOUT ID
04
05
06 FABRICATION NOTES
07 Component Designators
08
09
10
11 DESIGN INFORMATION
12 DIMENSIONS
13 Height Information
14
15 ASSEMBLY
16 SHEET

MULTI-LAYER HOLES

.Drawn	.Company		
.Engineer			
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B Size 1:1	Int-FPGA-Interface-2.0-Digital.PcbDoc	Sheet 1	of 1